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  - ☐ Fee Attached
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Date	November 28, 2005	Reg. No.	41,405

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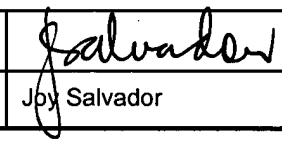
Signature			
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	Examiner: Rudy Zervigon
KRAMADHATI V. RAVI *et al.*	Art Unit: 1763
Application No.: 09/362,504	**APPELLANT'S BRIEF UNDER 37 CFR § 1.192**
Filed: July 27, 1999	
For: METHOD FOR REDUCING THE INTRINSIC STRESS OF HIGH DENSITY PLASMA FILMS	

MAIL STOP APPEAL BRIEF - PATENTS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants, in the above-captioned patent application, appeal the final rejection of claims 16-36. The claims on appeal have been finally rejected pursuant to MPEP § 706.07(b). Accordingly, this appeal is believed to be proper. This application was previously appealed, and was subsequently remanded to the Examiner on September 30, 2003.

I. REAL PARTY IN INTEREST:

The real party in interest for the above-identified application is APPLIED MATERIALS, INC., a Delaware corporation having its principal place of business at P.O. Box 450A, Santa Clara, California 95052. The assignment is recorded in the U.S. Patent and Trademark Office on October 16, 1996 at Reel 8331/Frame 0398.

II. RELATED APPEALS AND INTERFERENCES:

There are no appeals or interferences related to the present appeal.

III. STATUS OF CLAIMS:

Claims 16-36 are pending.

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al. Claims 17-19, 31, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. (US 4,500,408) in view of Onuki et al. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (US 5,772,771) in view of Onuki et al. Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. and Onuki et al. in view of Boys et al. Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Onuki et al. in view of Matsuura (US 5,319,247). Claims 25-30 and 33-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. and Onuki et al. in view of Li et al.

IV. STATUS OF AMENDMENTS:

On June 27, 2005, Applicants filed a Response to Office Action under 37 C.F.R. § 1.116 dated April 28, 2005. In an Advisory Action dated July 12, 2005, the Examiner maintained the rejection of all pending claims.

In accordance with 37 C.F.R. § 1.192(c)(9), a copy of the claims involved in the appeal are contained in the Appendix attached hereto.

V. SUMMARY OF CLAIMED SUBJECT MATTER:

This application discloses an integrated circuit formed on a semiconductor substrate, in which a layer of reduced stress if formed on the substrate. It further discloses a substrate processing system and a computer readable storage medium having program code for controlling the substrate processing system for processing the semiconductor substrate.

Independent Claim 16

In the embodiment of claim 16, an integrated circuit such as the circuit 800 shown in Fig. 6 is formed according to the method illustrated in Fig. 3. The method includes forming a plasma from a process gas by coupling sputtering energy into the substrate processing chamber (step 260); maintaining the plasma to deposit a first layer of film (stress reduction layer SRL)

over the substrate by sputtering without biasing the plasma toward the substrate (step 280); thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the substrate processing chamber and biasing the plasma toward the substrate (step 300) to deposit a second layer of the film (dielectric layer) over the first layer (step 320). See specification at page 10, line 18 to page 11, line 3.

Independent Claim 17 and Dependent Claims 18, 19, and 26-31

In the embodiment of claim 17, a substrate processing system 5 shown in Figs. 1 and 2 includes a housing 18 for forming a vacuum chamber 10; a vacuum pump 12 for evacuating the vacuum chamber; a pedestal 44, located within the housing 18, configured to hold a substrate 45; a gas distribution system (14, 16, 27, 29) fluidly coupled to the vacuum chamber 10; a plasma generation system (24, 26, 32, 34, 36, 38, 44, 50, 52) for forming a plasma from process gas within the vacuum chamber and for selectively biasing the plasma toward the substrate; a controller 31 for controlling the vacuum pump, the gas distribution system, and the plasma generation system; a memory 33 coupled to the controller for storing a program for directing the operation of the system. The program includes a set of instructions for depositing a film by, first, controlling the gas distribution system to introduce the process gas into the chamber (step 240); second, controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into the vacuum chamber (step 260) and deposit a first layer of the film over the substrate by sputtering without biasing the plasma towards the substrate (step 280); and third, controlling the plasma generation system to maintain the plasma by maintaining coupling of the sputtering energy into the vacuum chamber and bias the plasma toward the substrate (step 300) to deposit a second layer of the film over the first layer (step 320). See Fig. 3; and specification at page 5, line 21 to page 7, line 11; page 7, line 28 to page 8, line 5; and page 10, line 18 to page 11, line 3.

In the embodiment of claim 18, which recites depositing a plurality of first layers and second layers, multiple alternating (first) SRL and (second) bulk layers are deposited to form a "sandwiched" film as shown in Fig. 4, where bulk layers 420, 440, and 460 are "sandwiched" between SRLs 410, 430, 450, and 470. See specification at page 11, lines 25-31.

In the embodiment of claim 19, the gas distribution system includes sources of silicon and oxygen. See specification at page 10, lines 3-5.

In the embodiment of claim 25, the plasma is inductively coupled plasma. See specification at page 10, lines 18-10.

In the embodiment of claim 26, the inductively coupled plasma is formed from the process gas using only RF energy applied to a coil 26 disposed about the processing chamber 10. See specification at page 10, lines 18-21.

In the embodiment of claim 27, the substrate processing chamber is a high-density plasma chemical vapor deposition chamber and the inductively coupled plasma is a high density plasma. See specification at page 7, lines 12-17.

In the embodiment of claim 29, the process gas introduced by the gas distribution system includes flows of silicon and oxygen. See specification at page 10, lines 3-5.

In the embodiment of claim 30, the plasma generating system includes a first electrode 24, a second electrode included in the pedestal 44, and a coil 26 disposed about the vacuum chamber 10. See specification at page 6, lines 10-14 and lines 18-24.

In the embodiment of claim 28, the substrate 45 is disposed on the second electrode (pedestal 44) and electric energy is applied to the first and second electrodes while maintaining the application of the RF energy. See specification at page 8, lines 26-30.

In the embodiment of claim 31, the source of silicon contains silane. See specification at page 10, lines 3-4.

Independent Claim 20 and Dependent Claims 21 and 22

In the embodiment of claim 20, a high-density plasma chemical vapor deposition system 5 shown in Figs. 1 and 2 includes a housing 18 for forming a vacuum chamber 10; a pedestal 44, located within the housing 18, configured to hold a substrate 45; means (14, 16, 27, 29) for introducing reactants into the vacuum chamber 10; means (26, 32, 34) for generating a plasma from the reactants by applying a sputtering power to the reactants to deposit a first layer of a film (SRL 205) on the substrate during a first time period, the first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film (bulk film layer 210);

means (24, 36, 38, 44, 50, 52) for biasing the plasma toward the substrate 45 during a second time period after the first time period to enhance a sputtering of the plasma while maintaining application of the sputtering power to the reactants and deposit the subsequent layer. See steps 260-320 in Fig. 3; specification at page 5, line 21 to page 7, line 11; page 7, line 28 to page 8, line 5; page 8, lines 23-30; and page 10, line 18 to page 11, line 3.

In the embodiment of claim 21, the apparatus further includes means (12, 12a) for maintaining a pressure of between about 0.001-10 torr in the vacuum chamber 10 while the films are deposited. See specification at page 5, line 23; and page 10, lines 12-15.

In the embodiment of claim 22, the apparatus further includes means (44) for maintaining a wafer temperature of between about 100-500°C in the vacuum chamber 10 while the films are deposited. See specification at page 6, lines 2-4; an page 10, lines 15-17.

Independent Claim 23 and Dependent Claims 24 and 36

In the embodiment of claim 23, an integrated circuit, such as the circuit 800 shown in Fig. 6, includes a plurality of active devices (803, 806) formed in the semiconductor substrate; at least one metal layer (M1) formed above the semiconductor substrate; and at least one insulating layer (PMD 821) formed between the metal layer and the semiconductor substrate. The insulating layer has a plurality of patterned holes filled with electrically conductive material (826) to electrically connect selected portions of the metal layers to selected portions of the semiconductor substrate. The insulating layer includes a first silicon oxide layer (SRL 205) and a second silicon oxide layer (bulk film layer 210). The first and second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, the first silicon oxide layer deposited for the reduction of mechanical stress in the second silicon oxide layer. See specification at page 13, lines 5-27.

In the embodiment of claim 24, the integrated circuit further includes a second metal layer (M2) formed above the semiconductor substrate and below the at least one insulating layer (IMD2); a second insulating layer (IMD1) formed between the second metal layer (M2) and the semiconductor substrate; the second insulating layer (IMD1) having a second plurality of patterned holes filled with electrically conductive material (826) to electrically connect selected

portions of the second metal layer (M2) to selected areas of the plurality of active devices. See specification at page 13, lines 5-27.

In the embodiment of claim 36, the first silicon oxide layer (SRL 205) is deposited on the substrate by placing the substrate in a process chamber and applying a sputtering power to reactants to generate a plasma in the process chamber, and the second silicon oxide layer (bulk film layer 210) is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants. See specification at page 7, line 28 to page 8, line 5.

Independent Claim 32 and Dependent Claims 33-35

In the embodiment of claim 32, a computer readable storage medium has program code for controlling a substrate processing system. The program code includes a first set of computer instructions for controlling the gas delivery system to introduce a process gas into the processing chamber 10; a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into the processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing the plasma towards the substrate; and a third set of computer instructions for controlling the plasma generation system to maintain the plasma by maintaining coupling of the sputtering energy into the processing chamber and to bias the plasma toward the substrate to deposit a second layer of the film over said first layer. See steps 240-320 of Fig. 3; and specification at page 10, line 12 to page 11, line 3.

In the embodiment of claim 33, the plasma is an inductively coupled plasma. See specification at page 10, lines 18-10.

In the embodiment of claim 34, the substrate processing system is a high density plasma system. See specification at page 7, lines 12-17.

In the embodiment of claim 35, the process gas includes flows of silicon and oxygen. See specification at page 10, lines 3-5.

VI. GROUNDS OF REJECTION PRESENTED FOR REVIEW:

A. Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al.

B. Claims 17-19, 31, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. (US 4,500,408) in view of Onuki et al.

C. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (US 5,772,771) in view of Onuki et al.

D. Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. and Onuki et al. in view of Boys et al.

E. Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Onuki et al. in view of Matsuura (US 5,319,247).

F. Claims 25-30 and 33-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. and Onuki et al. in view of Li et al.

VII. ARGUMENTS:

A. Claim 16 is not properly rejected under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over, Onuki et al.

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over, Onuki et al. Onuki et al. does not disclose or suggest every element of claim 16.

Onuki et al. discloses a switching bias sputtering process whereby d.c. sputtering and d.c. bias sputtering are operated alternately (page 182, right column, lines 9-11). As illustrated in Figs. 1 and 2, the switching bias sputtering process involves alternating step pulses of sputtering power and bias voltage. The step pulses of sputtering power and bias voltage alternate, and do not overlap in time. The use of the switching bias sputtering method is intended to enhance the step coverage and quality of Al films (page 182, right column, lines 12-13).

In rejecting the claims, the Examiner relies on Onuki et al. for allegedly disclosing maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al., however, specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner points to Fig. 1(a) in Onuki et al. for the disclosure of maintaining the application of the sputtering power while biasing the plasma toward the substrate. The Examiner asserts that Onuki et al teach the method limitations of claim 16 with reference to Fig. 1a,b. Fig. 1a,b teach both zero and non-zero bias voltages repeated between 1 and 18 cycles providing multiple layers (Section 2.1).

Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Fig. 1b clearly shows **no** overlap between the bias voltage and the sputtering power. Fig. 1a merely shows a conventional DC sputtering with 4kW sputtering power and zero bias voltage, and conventional DC bias sputtering with 4kW sputtering power and –200V bias voltage. Nothing in Onuki et al., however, teaches or suggests combining or alternating the conventional DC sputtering and DC bias sputtering. As to the 18 cycles mentioned in the Examiner's statement, Onuki et al. actually states: "In the case of one-step switching bias sputtering, a cycle consisted of 5 s d.c. and 5 s d.c. bias sputtering. A cycle was repeated 18 times for the formation of 0.5 μm thick Al-0.5wt.%Cu-1wt.%Si films." This relates to the one-step switching bias sputtering shown in Fig. 1b in which there is **no** overlap between the sputtering power and the bias voltage. It has nothing to do with the conventional DC sputtering and conventional DC bias sputtering shown in Fig. 1a.

The Examiner misconstrues Onuki et al., including the teachings of Fig. 1a,b, to arrive at the erroneous conclusion that Onuki et al. anticipates or renders obvious claim 16. Claim 16 recites depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. Onuki et al. clearly does not teach depositing the two different layers. Nor does Onuki et al. recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress

of films deposited on the substrate (Page 4, lines 1-3 and Abstract). Therefore, claim 16 is novel and patentable over Onuki et al.

The Examiner makes the conclusory allegation that Onuki et al., taken as a whole, teaches that it would have been obvious to apply its conventional sputtering recursively as shown in Figure 1b, and states: "Motivation for a person of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b is for controlling the argon content in the deposited films as taught by Onuki (left column; Page 184)." *This, however, does not address the problem that Onuki et al. does not disclose or suggest maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer.*

In response to Applicants' argument that Fig. 1b of Onuki et al. clearly shows no overlap between the bias voltage and the sputtering power, the Examiner asserts that at a minimum, Onuki's disclosure taken as a whole teaches that it would have been obvious to one of ordinary skill in the art to apply Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b.

The lack of overlap in Fig. 1b of Onuki et al. supports Applicants' argument that the claims are patentable because, for instance, the references do not teach or suggest maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. This is demonstrated by the fact that there is no overlap between the bias voltage and the sputtering power in Figure 1b.

In response to Applicants' argument that Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage, the Examiner states that

the right portion of Onuki's Figure 1a shows applying sputtering power and bias voltage at the same time.

The Examiner's statement is inapposite. The Examiner relies on the switching bias sputtering Figure 1b in Onuki et al. for allegedly disclosing the claimed feature. On the other hand, Figure 1a shows conventional DC sputtering and conventional DC bias sputtering. The Examiner alleges: "It is not clear in Jim Onuki's Figure 1a and accompanying text that Onuki's conventional sputtering is one complete process, distinct processes, or is a process applied recursively. However, Jim Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b." Onuki et al. discloses switching bias sputtering (Figure 1b) in contrast with conventional sputtering (Figure 1a). Nothing in Onuki et al. suggests the recursive conventional sputtering process proposed by the Examiner.

B. Claims 17-19, 31, and 32 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. (US 4,500,408) in view of Onuki et al.

Claims 17-19, 31, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. (US 4,500,408) in view of Onuki et al. The Examiner recognizes that Boys et al. does not teach sputtering without biasing plasma toward the substrate. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

The Examiner alleges: "Applicant states that neither Onuki nor Boys teach depositing plural layers of thin films." Applicants did not make such a statement. Applicants did state: "Boys et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma."

In addition, claim 18 further recites that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached. The references do not disclose or suggest depositing a plurality of first layers by sputtering without biasing the plasma and second layers by sputtering and biasing the plasma. Claim 19 depends from claim 17 and further recites silicon and oxygen in the process gas. Claim 31 depends from claim 19 and further recites that the source of silicon contains silane.

For at least the foregoing reasons, Applicants respectfully submit that independent claim 17 and claims 18, 19, and 31 depending therefrom are patentable.

Applicants respectfully assert that independent claim 32 is patentable over the cited references because, for instance, they do not teach or suggest a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into said processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing said plasma towards said substrate; and a third set of computer instructions for controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said processing chamber and to bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

The Examiner recognizes that Boys et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

For at least the foregoing reasons, Applicants respectfully submit that claim 32 is patentable.

In response to Applicants' argument that claim 32 is patentable because neither Boys et al. nor Onuki et al. discloses or suggests a controller or a memory storing a program for

directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma, the Examiner states: "That Onuki and Boys et al are not clear in teaching ' . . . deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma . . .' is well established. The Examiner has proposed a 102(b)/103(a) rejection in this regard in view of Onuki solely."

C. Claim 20 is not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (US 5,772,771) in view of Onuki et al.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (US 5,772,771) in view of Onuki et al. The Examiner recognizes that Li et al. do not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. For at least the foregoing reasons, claim 20 is patentable.

D. Claims 21 and 22 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al., and Onuki et al. in view of Boys et al.

Claims 21 and 22 depend from claim 20, and stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al., and Onuki et al. in view of Boys et al. The Examiner cites Boys et al. for allegedly disclosing temperature and pressure control means. Boys et al., however, does not cure the deficiencies of Li et al. and Onuki et al., since Boys et al. also fails to teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. Accordingly, claims 21 and 22 are patentable.

E. Claims 23, 24, and 36 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Onuki et al. in view of Matsuura (US 5,319,247)

Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Onuki et al. in view of Matsuura (US 5,319,247).

Applicants respectfully assert that claim 23 is patentable over the references because, for instance, the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate and including a first silicon oxide layer and a second silicon oxide layer deposited using a high-density plasma chemical vapor deposition process, where the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness, since the Examiner has not pointed to anything in the references that would suggest the claimed invention. Onuki et al. does not teach depositing silicon oxide layers. Matsuura discloses silicon oxide layers, but fails to teach or suggest a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer.

With regard to the rejection of claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Onuki et al. in view of Matsuura, the Examiner alleges that "the sole difference between the claimed invention and the above conveyed prior art is the lack of intended use in Applicant's product claim." The claim limitation at issue is "at least one insulating layer formed between said metal layer and said semiconductor substrate, said insulating layer having a plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said metal layer to selected portions of said semiconductor substrate, wherein said insulating layer comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer." The Examiner has not pointed to anything in the references that would suggest the claimed invention. Onuki et al. does not teach depositing silicon oxide layers. Matsuura discloses silicon oxide layers, but fails to teach

or suggest a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer.

Although Onuki et al. at Fig. 4 shows a SiO_2 layer, it is "thermally grown," not by high-density plasma chemical vapor deposition process. In addition, Onuki et al. does not teach or suggest two silicon oxide layers, wherein the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer. The references do not, individually or combined, teach or suggest depositing first and second silicon oxide layers by high-density plasma chemical vapor deposition, where a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer. The claim features not taught or suggested in Onuki et al. and Matsuura are not merely intended use features.

Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. The references are directed to very different processes for forming different films to achieve different purposes. For example, Onuki et al. is directed to forming sputtered Al and Al alloy films using switching bias sputtering involving d.c. sputtering and d.c. bias sputtering; while Matsuura relates to deposition of silicon oxide films by plasma CVD. There is no suggestion that the operating conditions for depositing silicon oxide layers in Matsuura can be combined with the switching bias sputtering technique taught in Onuki et al.

In addition, claim 24 further recites that a second metal layer is formed above the substrate and below the at least one insulating layer, and a second insulating layer is formed between the second metal layer and the substrate. Claim 36 further recites that the first silicon oxide layer is deposited on the substrate by applying a sputtering power to reactants to generate a plasma in a process chamber, and the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants. These features are also missing from the references.

For at least the foregoing reasons, Applicants respectfully assert that claim 23 and claims 24 and 36 depending therefrom are patentable.

F. Claims 25-30 and 33-35 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. and Onuki et al. in view of Li et al.

Claims 25-30 and 33-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boys et al. and Onuki et al. in view of Li et al. Li et al. is cited for allegedly disclosing plasma generation by an inductively coupled plasma.

Claims 25-30 depend from claim 17, and are submitted to be patentable at least due to their dependency from claim 17. Li et al. does not cure the deficiencies of Boys et al. and Onuki et al., since Li et al. also fails to teach depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

Claims 33-35 depend from claim 32, and are submitted to be patentable for at least the reasons that claim 32 is patentable as discussed above. For example, Li et al. does not disclose a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma.

X. CONCLUSION:

In view of the foregoing arguments distinguishing claims 16-36 over the art of record, Applicants respectfully submit that the claims are in condition for allowance, and respectfully request that the rejection of these claims be reversed.

Respectfully submitted,

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Encl.: Appendix of claims involved in appeal

CLAIMS APPENDIX

1.-15. (canceled)

16. (previously presented) An integrated circuit formed on a semiconductor substrate by the method of:

a) flowing a process gas into a substrate processing chamber;

b) forming a plasma from said process gas by coupling sputtering energy into said substrate processing chamber;

c) thereafter, maintaining said plasma to deposit a first layer of a film over said substrate by sputtering without biasing said plasma toward said substrate; and

d) thereafter, maintaining said plasma by maintaining coupling of said sputtering energy into said substrate processing chamber and biasing said plasma toward said substrate to deposit a second layer of said film over said first layer.

17. (previously presented) A substrate processing system comprising:

a housing for forming a vacuum chamber;

a vacuum pump for evacuating said vacuum chamber;

a pedestal, located within said housing, configured to hold a substrate;

a gas distribution system fluidly coupled to said vacuum chamber;

a plasma generation system for forming a plasma from process gas within said vacuum chamber and for selectively biasing said plasma toward said substrate;

a controller for controlling said vacuum pump, said gas distribution system and said plasma generation system;

a memory coupled to said controller and storing a program for directing the operation of said system, said program including a set of instructions for depositing a film by

first, controlling said gas distribution system to introduce said process gas into said chamber;

second, controlling said plasma generation system to form a plasma from said process gas by coupling sputtering energy into said vacuum chamber and deposit a first layer of said film over said substrate by sputtering without biasing said plasma towards said substrate; and

third, controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

18. (previously presented) The substrate processing system of claim 17 wherein said program further includes instructions for depositing a plurality of said first layers and said second layers by

fourth, depositing a third layer of said film over said second layer by controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and stop biasing said plasma toward said substrate;

fifth, depositing a fourth layer of said film over said third layer by controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and bias said plasma toward said substrate; and

sixth, performing the second and third steps iteratively at least once until a desired thickness of said film is reached.

19. (previously presented) The apparatus of claim 17 wherein said gas distribution system includes sources of silicon and oxygen fluidly coupled to said gas distribution system.

20. (previously presented) A high-density plasma chemical vapor deposition system comprising:

a housing for forming a vacuum chamber;

a pedestal, located within said housing, for holding a substrate;

means for introducing reactants into said vacuum chamber;

means for generating a plasma from said reactants by applying a sputtering power to said reactants to deposit a first layer of a film on said substrate during a first time period, said first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film; and

means for biasing said plasma toward said substrate during a second time period after said first time period to enhance a sputtering of said plasma while maintaining application of said sputtering power to said reactants and deposit said subsequent layer.

21. (original) The apparatus of claim 20, further comprising means for maintaining a pressure of between about 0.001-10 torr in said vacuum chamber while said films are deposited.

22. (original) The apparatus of claim 20, further comprising means for maintaining a wafer temperature of between about 100-500°C in said vacuum chamber while said films are deposited.

23. (original) An integrated circuit formed on a semiconductor substrate, said integrated circuit comprising:

(a) a plurality of active devices formed in said semiconductor substrate;

(b) at least one metal layer formed above said semiconductor substrate; and

(c) at least one insulating layer formed between said metal layer and said semiconductor substrate, said insulating layer having a plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said metal layer to selected portions of said semiconductor substrate, wherein said insulating layer comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer.

24. (original) The integrated circuit of claim 23, further comprising:

(d) a second metal layer formed above said semiconductor substrate and below said at least one insulating layer;

(e) a second insulating layer formed between said second metal layer and said semiconductor substrate, said second insulating layer having a second plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said second metal layer to selected areas of said plurality of active devices.

25. (previously presented) The substrate processing system of claim 17 wherein said plasma is an inductively coupled plasma.

26. (previously presented) The substrate processing system of claim 25 wherein said inductively coupled plasma is formed from said process gas using only RF energy applied to a coil disposed about the processing chamber.

27. (previously presented) The substrate processing system of claim 25 wherein said substrate processing chamber is a high-density plasma chemical vapor deposition chamber and said inductively coupled plasma is a high density plasma.

28. (previously presented) The substrate processing system of claim 30 wherein the substrate is disposed on said second electrode and electric energy is applied to said first and second electrodes while maintaining the application of said RF energy.

29. (previously presented) The substrate processing system of claim 17 wherein said process gas introduced by said gas distribution system includes flows of silicon and oxygen.

30. (previously presented) The processing system of claim 17 wherein said plasma generating system includes a first electrode, a second electrode, and a coil disposed about the vacuum chamber, wherein said pedestal includes said second electrode.

31. (previously presented) The substrate processing system of claim 19 wherein said source of silicon contains silane.

32. (previously presented) A computer readable storage medium having program code embodied therein, said program code for controlling a substrate processing system, wherein said substrate processing system includes a processing chamber, a gas delivery system, a plasma generation system and a controller configured to control the gas delivery system and the plasma generation system said program code controlling the semiconductor processing system to process a wafer in the chamber in accordance with the following:

(i) a first set of computer instructions for controlling the gas delivery system to introduce a process gas into the processing chamber;

(ii) a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into said processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing said plasma towards said substrate; and

(iii) a third set of computer instructions for controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said processing chamber and to bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

33. (previously presented) The computer readable storage medium of claim 32, wherein said plasma is an inductively coupled plasma.

34. (previously presented) The computer readable storage medium of claim 33 wherein said substrate processing system is a high density plasma system.

35. (previously presented) The computer readable storage medium of claim 32 wherein said process gas includes flows of silicon and oxygen.

36. (previously presented) The integrated circuit of claim 23 wherein the first silicon oxide layer is deposited on the substrate by placing the substrate in a process chamber and applying a sputtering power to reactants to generate a plasma in the process chamber, and wherein the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.